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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/531,135	03/17/2000	Tohru Watanabe	005586-20035	5243
26021	7590	02/01/2006	EXAMINER	
HOGAN & HARTSON L.L.P. 500 S. GRAND AVENUE SUITE 1900 LOS ANGELES, CA 90071-2611			MISLEH, JUSTIN P	
			ART UNIT	PAPER NUMBER
			2612	

DATE MAILED: 02/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/531,135	WATANABE, TOHRU	
	<b>Examiner</b>	<b>Art Unit</b>	
	Justin P. Misleh	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 14 July 2005 AND 03 January 2006.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1 - 11 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) 2 - 6 and 8 -10 is/are allowed.  
 6) Claim(s) 1,7 and 11 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 14 July 2005 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### *Response to Amendments/Arguments*

1. Upon closer inspection of claim amendments to the independent Claims 1, 7, and 11, submitted July 14, 2005, the Examiner has become aware of additional issues. It is now believed that the claims were amended in such a way that each amended independent claim fails to meet the particular requirement of 35 U.S.C. 112, 1<sup>st</sup> paragraph, pertaining to new matter.

Accordingly, this Office Action is made Final and succeeds the previous Final Office (mailed October 5, 2005).

2. However, Applicant's arguments filed January 3, 2005 have been fully considered but they are not persuasive.

3. Applicant argues, "Yamanaka discloses a configuration in which pixel mixing is performed using odd line data and even line data. However, nowhere does the reference disclose or suggest adding information charges accumulated in the odd and even lines and, after further accumulating information charges in the odd and even lines, adding the information charges further accumulated in the odd lines and the previously added charges. Accordingly, the invention defined by claims 1, 7 and 11 is not anticipated by Yamanaka et al."

4. The Examiner respectfully disagrees with Applicant's position. As best ascertained by the Examiner, the last paragraph of amended Claims 1, 7, and 11 pertain to figures 3 and 6 – 8 of Applicant's present invention. According to page 17 (lines 3 – 5) of the disclosure, "image data D1' and D2' are added together at the adder 26 where a third image data D3 is output." The previous Office Action (see page 4) noted Yamanaka actually discloses Applicant's invention in

figures 2D and 2E and columns 3 (lines 17 – 33) and 8 (lines 17 – 22). Yamanaka clearly shows image data from odd and even lines corresponding to first and second image being added together to output third and fourth image data.

5. For these reasons, the Examiner deems the rejections in view of Yamanaka are proper, and have been maintained.

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. **Claims 1, 7, and 11** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

As set forth in Claims 1, 7, and 11, after information charges are accumulated in the first and second light receiving pixels, the accumulated charges in those pixels are added together. Subsequently, after performing further accumulation of information charges in the first and second light receiving pixels, the information charges further accumulates in the first light receiving pixels are added together with previously added charges.

However, as best ascertained by the Examiner, the recited portion of Claims 1, 7, and 11 pertains to figures 3 and 6 – 8 of Applicant's present invention. According to page 17 (lines 3 –

5) of the disclosure, “image data D1’ and D2’ are added together at the adder 26 where a third image data D3 is output.” Nowhere in the disclosure it is recited, suggested, or implied that the further accumulated first light receiving pixels are added together with previously added charges.

For the purposes of examination, the recited portion of Claims 1, 7, and 11 will be interpreted in accordance with page 17 (lines 3 – 5) of the disclosure.

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. **Claims 1, 7, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by**

Yamanaka et al.

10. For **Claim 1**, Yamanaka et al. disclose, as shown in figures 1, 2, and 4 and as stated in columns 6 (lines 16 – 67), a solid-state image pickup apparatus (see figure 1) comprising:

a solid-state image pickup device (11) in which a first light receiving pixel (EVEN) is disposed in a plurality of lines in one-line units (see figure 2A), and a second light receiving pixel (ODD) capable of being driven independently (see figures 2B, 2C, and 4 and column 6, lines 18 – 26) from said first light receiving pixel (EVEN) is disposed in at least one-line units between first light receiving pixels of the plurality of lines (see figure 2A);

a drive circuit (18; see figure 1) for driving the first and second light receiving pixels (EVEN and ODD) of said solid-state image pickup device (11) and accumulating information charges at mutually different times (see figures 4A and 4C) between first light receiving pixel (EVEN) and second light receiving pixel (ODD), as well as transferring and outputting information charges accumulated in said first and second light receiving pixels independently of each other (see figure 4C);

timing control circuit (20; see figure 1) for respectively setting the storage time of information charges at the first light receiving pixel (EVEN) and the storage time of information charges at the second light receiving pixel (ODD) of said solid-state image pickup device (1); and

a signal processing circuit (24; see figure 1) for generating an image signal by adding a first output corresponding to the first light receiving pixel and a second output corresponding to the second light receiving pixel of said solid-state image pickup device (see figures 2D, 2E, and 4G);

wherein after driving the first and second light receiving pixels (EVEN and ODD) to accumulate information charges in the first and second light receiving pixels (EVEN and ODD), the drive circuit (18; see figure 1) adds information charges accumulated in the first light receiving pixel (EVEN) to information charges accumulated in the second light receiving pixel (ODD), and, the drive circuit drives the first and second light receiving pixels to further accumulate information charges in the first and second light receiving pixels and further adds information charges thus accumulated in the first and second light receiving pixels (see

explanation below and additionally see figures 2D and 2E and also see column 3, lines 17 – 33, and column 8, lines 17 – 22).

As best ascertained by the Examiner, the last paragraph of amended Claims 1, 7, and 11 pertain to figures 3 and 6 – 8 of Applicant’s present invention. According to page 17 (lines 3 – 5) of the disclosure, “image data D1’ and D2’ are added together at the adder 26 where a third image data D3 is output.” The previous Office Action (see page 4) noted Yamanaka actually discloses Applicant’s invention in figures 2D and 2E and columns 3 (lines 17 – 33) and 8 (lines 17 – 22). Yamanaka clearly shows image data from odd and even lines corresponding to first and second image being added together to output third and fourth image data.

11. For **Claim 7**, a solid-state image pickup apparatus (see figure 1) comprising:

a solid-state image pickup device (11) having a line of first light receiving pixels (EVEN) and a line of second light receiving pixels (ODD) disposed so as to respectively correspond to horizontal scanning lines (see figure 2) and capable of being driven independently (see figures 2B, 2C, and 4 and column 6, lines 18 – 26) from each other said first light receiving pixels (EVEN) and said second light receiving pixels (ODD);

a drive circuit (18; see figure 1) for driving the first and second light receiving pixels (EVEN and ODD) of said solid-state image pickup device (11) and accumulating information charges at mutually different times (see figures 4A and 4C) between first light receiving pixel (EVEN) and second light receiving pixel (ODD), as well as transferring and outputting information charges accumulated in said first and second light receiving pixels independently of each other (see figure 4C) and generating a first output according to said information charges

accumulated in said first light receiving pixels (see figure 4D) and a second output according to said information charges accumulated in said second light receiving pixels (see figure 4D); and a signal processing circuit (24; see figure 1) for generating an image signal by adding together the first output and the second output corresponding to identical horizontal scanning lines (see figures 2D, 2E, and 4G);

wherein after driving the first and second light receiving pixels (EVEN and ODD) to accumulate information charges in the first and second light receiving pixels (EVEN and ODD), the drive circuit (18; see figure 1) adds information charges accumulated in the first light receiving pixel (EVEN) to information charges accumulated in the second light receiving pixel (ODD), and, the drive circuit drives the first and second light receiving pixels to further accumulate information charges in the first and second light receiving pixels and further adds information charges thus accumulated in the first and second light receiving pixels (see explanation below and additionally see figures 2D and 2E and also see column 3, lines 17 – 33, and column 8, lines 17 – 22).

As best ascertained by the Examiner, the last paragraph of amended Claims 1, 7, and 11 pertain to figures 3 and 6 – 8 of Applicant’s present invention. According to page 17 (lines 3 – 5) of the disclosure, “image data D1’ and D2’ are added together at the adder 26 where a third image data D3 is output.” The previous Office Action (see page 4) noted Yamanaka actually discloses Applicant’s invention in figures 2D and 2E and columns 3 (lines 17 – 33) and 8 (lines 17 – 22). Yamanaka clearly shows image data from odd and even lines corresponding to first and second image being added together to output third and fourth image data.

12. For **Claim 11**, Yamanaka et al. disclose, as shown in figures 1, 2, and 4 and as stated in columns 6 (lines 16 – 67), a solid-state image pickup apparatus (see figure 1) comprising:

a solid-state image pickup device (11) in which a first light receiving pixel (EVEN) is disposed in a plurality of lines in one-line units (see figure 2A), and a second light receiving pixel (ODD) capable of being driven independently (see figures 2B, 2C, and 4 and column 6, lines 18 – 26) from said first light receiving pixel (EVEN) is disposed in at least one-line units between first light receiving pixels of the plurality of lines (see figure 2A);

a drive circuit (18; see figure 1) for driving the first and second light receiving pixels (EVEN and ODD) of said solid-state image pickup device (11) and accumulating information charges at mutually different times (see figures 4A and 4C) between first light receiving pixel (EVEN) and second light receiving pixel (ODD);

timing control circuit (20; see figure 1) for respectively setting the storage time of information charges at the first light receiving pixel (EVEN) and the storage time of information charges at the second light receiving pixel (ODD) of said solid-state image pickup device (1); wherein

after driving the first and second light receiving pixels (EVEN and ODD) to accumulate information charges in the first and second light receiving pixels (EVEN and ODD), the drive circuit (18; see figure 1) adds information charges accumulated in the first light receiving pixel (EVEN) to information charges accumulated in the second light receiving pixel (ODD), and, the drive circuit drives the first and second light receiving pixels to further accumulate information charges in the first and second light receiving pixels and further adds information charges thus accumulated in the first and second light receiving pixels (see explanation below and

additionally see figures 2D and 2E and also see column 3, lines 17 – 33, and column 8, lines 17 – 22).

As best ascertained by the Examiner, the last paragraph of amended Claims 1, 7, and 11 pertain to figures 3 and 6 – 8 of Applicant’s present invention. According to page 17 (lines 3 – 5) of the disclosure, “image data D1’ and D2’ are added together at the adder 26 where a third image data D3 is output.” The previous Office Action (see page 4) noted Yamanaka actually discloses Applicant’s invention in figures 2D and 2E and columns 3 (lines 17 – 33) and 8 (lines 17 – 22). Yamanaka clearly shows image data from odd and even lines corresponding to first and second image being added together to output third and fourth image data.

*Allowable Subject Matter*

13. **Claims 2 – 6 and 8 – 10** are allowed.

14. The following is a statement of reasons for the indication of allowable subject matter:

While the closest prior art (Yamanka et al. and Yonemoto) discuss the particulars of the solid-state image pickup apparatus including first and second light receiving pixels, the independent accumulation of charge in the first and second light receiving pixels, the independent storage of charge of the accumulated first and second light receiving pixels, and the summing of the stored and accumulated charge of the first and second light receiving pixels, as required and discussed above in regards to Claims 1, 7 and 11;

The closest prior art does not teach or fairly suggest calculating a vertical transfer smear component on the basis of a ratio of said respective accumulation times of information charges at said first and second light receiving pixels and of a difference of said first and second outputs

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corresponding to said first and second light receiving pixels; does not teach or fairly suggest calculating a smear quantity generated during vertical transfer of said information charges on the basis of a ratio of said respective accumulation times of said information charges at said first and second light receiving pixels and of said first output and said second output; and does not teach or fairly suggest calculating smear quantity generated during vertical transfer of said information charges on the basis of a ratio of said respective accumulation times of said information charges at said first and second light receiving pixels and of said first output and said second output.

*Conclusion*

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 571.272.7313. The Examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

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If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Ngoc Yen Vu can be reached on 571.272.7320. The fax phone number for the organization where this application or proceeding is assigned is 571.273.3000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*JPM*  
*January 24, 2006*



NGOC-YEN VU  
PRIMARY EXAMINER